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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/059,644	Applicant(s) PAN, PAI-HUNG	
	Examiner Michael Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41 and 43-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41 and 43-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed on July 23, 2003. Claims 41 and 43-52 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

1. Claims 45-49 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

** Re base claim 45, original specification does not teach and support "the conductive gate structure comprising at least one metal-comprising material, an oxidation-resistant cap layer, and a conductive polysilicon layer", in which the oxidation-resistant cap layer is recited between the metal-comprising material and the conductive polysilicon layer. Indeed, as shown in Figure 1, the conductive gate structure 10 comprising at least one an oxidation-resistant cap layer 30 formed on the metal-comprising material 26.

(Dependent claims are rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 103

2. Claims 41,43,45,47, and 50 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Verhaar (5,015,598) with either Hiroki et al (5,512,771) or Kurimoto (5,306,655), and further of Pintchovski et al (5,126,283) and Park (5,545,578).

Verhaar teaches a method (at Figs 1-5; col 4, line 30 through col 5) for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate structure having a polysilicon gate electrode 12 formed on a gate oxide dielectric layer 11 formed on a semiconductor substrate 10 (col 4); forming barrier sidewall nitride spacers 20a directly adjacent (directly on or directly against) the sidewalls of the gate electrode 12 and joining the dielectric oxide layer 10 by anisotropically etching a silicon nitride layer 20 (col 4, lines 45-49; col 5, lines 10-52); and then oxidizing the substrate to channel oxidants through the gate dielectric layer 10

(col 5, lines 47-52) and underneath the spacers joined therewith and which is outwardly exposed laterally proximate the sidewall spacers, wherein only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is oxidized (Fig 5), while preventing oxidation of the upper parts of side faces of the gate electrode 12 by the action of the barrier insulating nitride spacers 10. Since Verhaar discloses forming the silicon nitride spacers 20a having a thickness between 15 and 50 nm and preferably close to 30 nm (col 4, lines 63-68) adjacent to the gate electrode 12; and since oxidizing at 900°C for a duration of 15 to 30 minutes in oxygen to form a silicon oxide layer 24 (fig 5) having a thickness of the order of 10 to 15 nm (100 to 150 Angstroms), only a portion only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is inherently oxidized and creating a "smiling gate" (can be seen by enlarging the gate electrode), wherein as shown from Figures 4 to 6 of Verhaar, after forming spacers 20a and prior to forming source and drain regions 22a,23a (Fig 6), exposing the substrate to oxidizing conditions to create a "smiling gate" (Figs 4-6). It is the fact that the present specification discloses (at page 7, lines 14-19) that only portion of the gate electrode is oxidized in a time period for growing "an oxide layer over a separate semiconductor substrate to a thickness of a round 80 Angstroms". Herein, since Verhaar grows a silicon oxide layer 24 having a thicker thickness of 100 to 150 Angstroms, only a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10, is inherently oxidized ("smiling gate"). Consequently, the burden shifted to applicant to demonstrate and prove that this apparent inherence does not in fact exist, In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138-139 (Fed. Cir. 1986).

In any event, as in the alternative under 103 rejection,: *Hiroki et al* '771 teach forming a "smiling gate" by oxidizing a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, wherein the oxide layer 6' underlying the silicon nitride spacer 7 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode of polysilicon material to form a "smiling gate" (col 12, lines 10-21; figs 6A-6B), wherein as shown from Figure 6A to Figure 6D of Hiroki, after forming spacers and prior to forming source and drain regions 3 (Fig 6D; col 12), the gate structure is exposed to oxidizing conditions to create a "smiling gate" (Figs 6B-6C), wherein the spacers protect at least

a portion of the polysilicon material of the gate electrode. *Kurimoto* teaches (at Figs 13a-13h; col 13, line 21 through col 16) forming a gate structure having a gate electrode 5f on a gate oxide dielectric layer 2 (figs 13a; col 13, lines 30+); forming barrier sidewall nitride spacers 10 over sidewalls of the gate electrode and joining the dielectric oxide layer 2 by anisotropically etching a silicon nitride layer 10 (figs 13C-13D); and then oxidizing by channeling oxidants through the dielectric layer, wherein only a portion of the gate electrode 5f, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 2 is oxidized during this oxidation due to the existence of nitride sidewall spacer 10 (col 13, lines 59-68) and insulating cap layer 9, wherein oxidants channels through the gate dielectric layer 2 and underneath the spacers joined therewith.

Therefore, it would have been obvious to one of ordinary skill in the art to create a "smiling gate" as taught by Hiroki and Kurimoto by oxidizing a portion of the gate electrode of Verhaar, wherein a portion of the oxide layer 11 underlying the spacers 20a as shown in figure 11 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode to form a "smiling gate". This is because of the desirability to have smaller gate-to-drain capacitance and thus to improve the speed of the circuit operation (col 8, lines 45-67; fig 2).

Verhaar thus lacks forming a gate structure comprising a polysilicon, a conductive reaction barrier metal nitride layer, and an overlying metal-comprising layer.

However, Pintchovski et al teach (at figs 3a-3c; col 5, line 60 through col 6, line 45) alternatively forming a gate electrode having a polysilicon layer 38, a conductive reaction barrier metal nitride layer 40, and an overlying metal 42. Similarly, Park et al teach (at Fig 1 col 1, lines 11-65; and Fig 4, col 4, line 25 through col 5) forming a gate structure comprising a polysilicon layer 14a (Fig 4G), an overlying metal-comprising layer 16a formed over the polysilicon layer 14a, and a top nitride cap layer 18a, wherein nitride sidewall spacers 22a are formed on sidewalls of the gate structure, wherein a only portion of the polysilicon layer 14a of the gate structure is oxidized (col 5, liens 3-14; Fig 1F).

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the gate structure of Verhaar by forming a multi-layered transistor gate electrode including a polysilicon material, a reaction barrier nitride, a

metal-comprising material, as taught by Pintchovski and Park. This is because of the desirability to fabricate high speed devices due to high conductivity of the multilayered gate electrode, wherein the conductive reaction barrier metal nitride layer also acts as a diffusion barrier.

3. Claims 44,48,49,51-52 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Verhaar (5,015,598) with either Hiroki '771 or Kurimoto '655, and further of Pintchovski '283 and Park '578, as applied above, and further of Brigham (5,714,413) and Kumagai (5,430,313).

The references including Verhaar and Kurimoto already teaches forming single sidewall barrier spacers over sidewalls of the gate (similarly to a first embodiment of the present invention as shown in figure 3 having a single sidewall barrier spacers 34).

The further main difference between the references applied above and the instant claim(s) is as follows: instead of using single sidewall spacers (first embodiment, fig 3 of present application), the present application, in a second embodiment (fig 5) and a third embodiment (fig 7), alternatively teaches using double sidewall spacers by etching first and second material layers.

However, Brigham teaches (at figs 2b-2c,3c; col 6, line 60 through col 7, line 6; cols 4-6) forming double sidewall spacers by depositing a second material layer on a first material layer and anisotropically etching the first and second layers to form double sidewall spacers, wherein Brigham expressly teaches "three or more layers of dielectric...are implemented to form a multi-layered spacer structures" (col 6, lines 1-6), and wherein silicon nitride is disclosed. Kumagai teaches (at figs 4B-4D; col 3, line 65 through col 4, line 15) forming single sidewall nitride spacers 16 on sidewalls of a gate 14, and alternatively, forming double sidewall nitride spacers including first sidewall nitride spacers 16 and second sidewall nitride spacers 30 by anisotropically etching a deposited first material barrier layer and then anisotropically etching a second deposited material barrier layer (figs 7A-7D; col 5, line 45 through col 6).

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Brigham, Kumagai, and Verhaar. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier mask during oxidation to form an oxide film.

This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate electrode.

Response to Arguments

4. Applicant's remarks filed July 23, 2003 have been fully considered but they are not persuasive in view of new ground(s) of rejection.

Applicant remarked at remark page 9 that "...Verhaar does not teach or suggest the claim 41 recited gate structure having a metal comprising material layer ..." and "...forming nitride comprising sidewall spacers directly on the gate sidewall....,the spacers contacting the metal-comprising material and polysilicon material.

In response, again, this is noted and found unconvincing. Under 35 USC 103 rejection, Pintchovski et al reference teaches the gate structure having a polysilicon layer 38, a conductive reaction barrier layer 40, and an overlying metal 42 (Figs 3a-3c; col 5, line 60 through col 6, line 45). Park also teaches forming the gate structure comprising a polysilicon layer, an overlying metal-comprising layer, an insulating cap layer, and nitride sidewall spacers directly on the sidewalls, wherein a portion of the polysilicon layer at the interface with the gate dielectric layer is oxidized. Thus, it would have been obvious to one of ordinary skill in the art to modify the gate structure of Verhaar by employing the gate structure having a polysilicon layer, a conductive reaction barrier layer, and an overlying metal, as combinatively taught by Pintchovski and Park, wherein nitride spacers are formed directly on the sidewalls of the gate structure as shown by Verhaar and Park. This is because of the desirability to fabricate high speed devices due to high conductivity of the gate electrode, wherein the conductive reaction barrier layer also acts as a diffusion barrier. The rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In Re Lyons 150 USPQ 741 (CCPA 1966). Applicant has argued and discussed the references individually without clearly addressing the combined teachings. It must be remembered that the references are relied upon in combination and are not meant to be considered separately as in a vacuum. It is the combination of all of the cited and relied upon references which make up the state of art with regard to the claimed invention. Applicant's claimed invention fails to patentably distinguish over the state of the art represented by the cited reference. It is well

settled that one can not show non-obviousness by attacking the references individually where, as here, the rejection is based on combinations of references. In re Young, 403 F.2d 754,159 USPQ 725 (CCPA 1968); In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Brigham and Kumagai are cited to show the formation of the single spacer, L-shaped double sidewall spacers by etching first and second material layers, and double sidewall spacers by depositing and anisotropically etching the first material layer and then depositing and anisotropically etching a second material layer. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Verhaar to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Brigham, Kumagai, and Verhaar. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier mask during oxidation to form an oxide film. This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate electrode. The rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In Re Lyons 150 USPQ 741 (CCPA 1966). It is well settled that one can not show non-obviousness by attacking the references individually where, as here, the rejection is based on combinations of references. In re Young, 403 F.2d 754,159 USPQ 725 (CCPA 1968); In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-01

Michael Trinh
Primary Examiner